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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,644	03/23/2004	Vahid Goudarzi	7463-44 (CE12694JME)	2480

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/806,644	GOUDARZI, VAHID	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claim 13 is objected to because of the following informalities: there is no antecedent basis for "the solder paste" or "the conductive runner". These terms are interpreted by the examiner to mean "the solder" and "the conductive areas", respectively, for the examination of this application. Appropriate correction is required.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 7, 9, 11, 12, 13, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suppelsa et al (U.S. Patent #5411199), in view of Economikos et al (U.S. Patent #5945735).

With respect to **claims 1, 2, and 7**, Suppelsa teaches applying solder onto conductive areas on the substrate (Fig. 4, 302 and Col 2 Ln 57-58), placing components onto the conductive areas for the components (Fig. 4, 304 and Col 2 Ln 60), a first reflow step (Fig. 4, 306), applying flux to the shield (Col 3 Ln 10-13), placing the shield over the solder cladded area (Fig. 4, 314), reflowing the assembly (Fig. 4, 316), cleaning the substrate after reflow (Fig. 4, 306 and Col 2 Ln 62-63), applying solder preforms onto conductive areas (Fig. 4, 302), but does

not teach a conductive shield track on the substrate or that a first reflow step provides a selectively solder cladded area over the conductive shield track. Economikos teaches a conductive shield track (Fig. 1, 19, 13, 23), and applying solder onto the conductive shield track (Fig. 1, 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to place a conductive shield track and solder on the substrate of Suppelsa as taught by Economikos, which would lead to the solder of Economikos being cladded before attaching the shield in the first reflow process of Suppelsa, in order to enhance the bond connection between the shield and the substrate.

With respect to **claims 9, 11, 12, and 17**, Suppelsa teaches circumscribing a predetermined area on the substrate with at least a portion of a metallized trace pattern (Fig. 4, 302), placing components on portions of the metallized trace pattern (Fig. 4, 304), placing the shield on the cladded trace pattern (Fig. 4, 314), reflowing the substrate (Fig. 4, 316), and that the step of applying solder comprises the step of applying solder paste to the metallized trace pattern (Fig. 4, 302), but does not teach applying solder to the metallized trace pattern, that reflowing the solder forms a cladded trace pattern on a portion of the metallized trace pattern reserved for the shield, or that the step of placing components comprises the step of placing a semiconductor die on portions of the metallized trace pattern. Economikos teaches applying solder on a portion of the metallized trace pattern reserved for the shield (Fig. 1, 15), and the placing of a semiconductor die on a portion the substrate (Fig. 1, 27). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to apply solder on the metallized trace pattern reserved for the shield as taught by Economikos, which would lead to the solder of Economikos being cladded in the first reflow step before attaching the shield in the final reflow process of Suppelsa, in order to enhance the bond connection between the shield and the substrate, and to have the step of placing components of Suppelsa comprise placing a semiconductor die on the metallized trace patterns as taught by Economikos in order to increase the functionality of the package.

With respect to **claims 13, and 16**, Suppelsa teaches solder applied onto conductive areas on the substrate (Fig. 4, 302), components placed onto the conductive areas for the components (Fig. 4, 304), that the solder applied to the conductive areas is reflowed (Fig. 4, 306), a metallic shield placed over the selectively solder cladded area, wherein the substrate including the shield over the selectively solder cladded area is reflowed (Fig. 4, 316), and that the solder applied onto the conductive areas is solder preforms (Fig. 4, 302), but does not teach solder applied to a conductive shield track, or that the first reflow step provides a selectively solder cladded area over the conductive shield track. Economikos teaches solder (Fig. 1, 15) applied to a conductive shield track (Fig. 1, 19, 13, 23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the substrate of Suppelsa with a conductive shield track and solder applied on the shield track, the solder being

selectively cladded by the first reflow step, in order to enhance the connection between the shield and the substrate.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suppelsa and Economikos, in view of Lee (U.S. Patent #5620927).

With respect to **claim 3**, Suppelsa and Economikos teach all of the limitations of claim 1, but do not teach that the step of applying flux comprises the step of picking up the shield and dipping the shield into the flux. Lee teaches a process in which a component is dipped into flux before it is reflowed (Col 3 Ln 65-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made apply the flux as in Suppelsa with the process of picking the shield up and dipping it into the flux as taught by Lee in order to remove oxides from the part to be connected by reflow.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suppelsa and Economikos, in view of Degani et al (U.S. Patent #5346118).

With respect to **claim 4**, Suppelsa and Economikos teach all of the limitations of claim 1, but do not teach that the step of applying solder paste onto the conductive shield track comprises the step of over printing the solder to increase the solder volume to the conductive shield track to accommodate for the shield's non-coplanarity. Degani teaches a process of overprinting the solder

paste in a connection (Col 4 Ln 15-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to overprint the solder applied on the conductive shield track as taught by Degani in order to achieve a satisfactory joint volume.

With respect to **claim 5**, Suppelsa and Economikos teach all of the limitations of claim 1, but do not teach that the step of placing components comprises the step of placing surface mount components onto the substrate. Degani teaches the placing of surface mount components onto a substrate (Col 1 Ln 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the step in Suppelsa of placing components on the substrate to be placing surface mounted components on the substrate as taught by Degani in order to secure the components to the substrate.

With respect to **claim 6**, Suppelsa and Economikos teach all of the limitations of claim 1, but do not teach that the step of applying solder comprises the step of applying solder paste onto the conductive areas forming conductive pads for the components and the shield track. Degani teaches that a step of applying solder to form conductive pads for component to be connected comprises applying solder paste (Col 4 Ln 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply solder paste to form conductive pads as taught by Degani in the step of applying solder in Suppelsa in order to enhance the connection between the components and shield track and the substrate.

With respect to **claim 10**, Suppelsa and Economikos teach all of the limitations of claim 9, but do not teach that the step of applying solder comprises the step of applying solder paste to the metallized trace pattern. Degani teaches that a step of applying solder to form conductive pads for component to be connected comprises applying solder paste (Col 4 Ln 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply solder paste to form conductive pads as taught by Degani in the step of applying solder in Suppelsa in order to enhance the connection between the components and the substrate.

With respect to **claim 14**, Suppelsa and Economikos teach all of the limitations of claim 13, but do not teach that the step of placing components comprises the step of placing surface mount components onto the conductive areas. Degani teaches the placing of surface mount components onto a substrate (Col 1 Ln 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the step in Suppelsa of placing components on the substrate to be placing surface mounted components on the conductive areas as taught by Degani in order to secure the components to the substrate.

With respect to **claim 15**, Suppelsa and Economikos teach all of the limitations of claim 13, but do not teach that the step of applying solder comprises the step of applying solder paste onto the conductive areas. Degani teaches that a step of applying solder to form conductive pads for component to

be connected comprises applying solder paste (Col 4 Ln 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply solder paste to the conductive areas as taught by Degani in the step of applying solder in Suppelsa in order to enhance the connection between the components and shield track and the substrate.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suppelsa and Economikos, in view of Liebman et al (U.S. Patent #5167361).

With respect to **claim 8**, Suppelsa and Economikos teach all of the limitations of claim 1, but do not teach that the step of applying solder comprises the step of screen printing solder paste onto the conductive areas. Liebman teaches that a step of applying solder can comprise screen printing solder paste onto circuitry (Col 2 Ln 29-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the step of applying solder in Suppelsa comprise screen printing solder paste onto the conductive areas as taught by Liebman in order to facilitate a connection between the components and the conductive areas.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bps

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